Abstract of the Disclosure:

A method for writing and reading data is performed on a dynamic memory circuit. The memory circuit has memory cells that can be addressed via word lines and bit lines. A word line is activated in the event of addressing of a memory area with a specific address. A word line has a plurality of mutually separate word line sections. Via the bit lines, in the event of addressing with the specific address, in parallel, a first number of data can be written to memory cells addressed by the address or the first number of data can be read from memory cells addressed by the address. In the event of addressing with a specific address, only a portion of the word line sections are activated, in order that only a portion of the memory cells connected to the word line are written to in parallel or read from in parallel.

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